What is claimed is:

1. An output buffer, comprising:

a first stage and a second stage, the first and second stages having outputs connected parallel to one another, the first stage providing buffer strength when a first stage enable signal is active, and the second stage providing buffer strength when a second stage enable signal is active.

2. The output buffer of claim 1, wherein the first and the second stages are additive when both are enabled.

3. The output buffer of claim 1, wherein each output stage comprises:

a complementary metal oxide semiconductor (CMOS) structure having a p-channel MOS device and an n-channel MOS device;

an AND gate having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to a data signal and another input connected to one of a plurality of enable signals; and

an OR gate having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to the data signal and another input connected to a complement of the one of the plurality of enable signals.

4. The output buffer of claim 3, and further comprising:

a bank of latches, the bank of latches having an enable latch and two or more trim latches, each trim latch storing a value representative of an enable signal, each trim latch connected to the respective enable input of one the plurality of output stages to provide its enable signal to its respective output stage.

5. The output buffer of claim 4, wherein each output stage further comprises:

a second CMOS structure substantially identical to the first CMOS structure, the second CMOS AND gate inputs connected to the data signal and to

one of a plurality of hard coded enable signals, and the second CMOS OR gate inputs connected to the data signal and to a complement of the one of the plurality of hard coded enable signals.

6. The output buffer of claim 5, and further comprising:

an output buffer selection circuit, comprising an OR gate connected to the enable latch output and to a general enable signal, the OR gate output connected to the complement of the enable signal to enable a predetermined output buffer strength when either the enable latch output or the general enable signal are active.

7. The output buffer of claim 1, and further comprising an output buffer trim circuit, the trim circuit comprising:

a bank of latches, the bank of latches having an enable latch and a plurality of trim latches, each trim latch storing a value representative of an enable signal, each trim latch connected to a respective enable input of one the plurality of output stages to provide its enable signal to its respective output stage.

8. An output buffer, comprising:

at least two parallel buffer stages, each stage activated upon receipt of a respective stage enable signal, the stages providing a range of output buffer strengths cumulatively to a total output buffer strength.

9. The output buffer of claim 8, wherein each output stage comprises:

a pair of CMOS components, the first CMOS component connected to a hard coded buffer strength signal, and the second CMOS component connected to a selectable buffer strength signal; and

selection circuitry to select either the first CMOS component or the second CMOS component.

10. The output buffer of claim 9, and further comprising:

selection circuitry to select either the first CMOS component or the second CMOS component.

11. The output buffer of claim 10, wherein the selection circuitry comprises:

a bank of latches, the bank of latches providing a plurality of enable signals, each enable signal for one of the second CMOS components of the plurality of the stages; wherein the bank of latches further comprises an enable latch to enable the plurality of enable signals.

12. An output buffer circuit, comprising:

a first output buffer stage for providing an output buffer strength in response to a first stage enable signal; and

at least one second output buffer stage, wherein each second output buffer stage is adapted to selectively provide additional buffer strength in response to a respective second stage enable signal.

13. The output buffer circuit of claim 12, wherein each output stage comprises:

a pair of CMOS components, the first CMOS component connected to a hard coded buffer strength signal, and the second CMOS component connected to a selectable buffer strength signal; and

selection circuitry to select either the first CMOS component or the second CMOS component.

14. An output buffer circuit, comprising:

a plurality of output stages, each output stage selectable to provide a component of a total output buffer strength, each output stage comprising:

a pair of CMOS components, the first CMOS component connected to a hard coded buffer strength enable signal, and the second CMOS component connected to a selectable buffer strength enable signal; and

selection circuitry to select either the first CMOS component or the second CMOS component.

15. The output buffer of claim 14, wherein the selection circuitry comprises:

a bank of latches, the bank of latches providing a plurality of enable signals, each enable signal for one of the second CMOS components of the plurality of the stages; and

wherein the bank of latches further comprises an enable latch to enable the plurality of enable signals.

16. An output buffer, comprising:

a first stage and a second stage, the first and second stages parallel to each other, the first stage comprising:

a first stage complementary metal oxide semiconductor (CMOS) structure having a p-channel MOS device and an n-channel MOS device;

a first OR gate having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to a data signal and another input connected to an enable signal; and

a first AND gate having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to the data signal and another input connected to the enable signal; and

the second stage comprising:

a second stage CMOS structure having a p-channel MOS device and an n-channel MOS device;

a second OR gate having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to a data signal and another input connected to an enable signal; and

a second AND gate having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to the data signal and another input connected to the enable signal.

17. The output buffer of claim 16, and further comprising:

an output buffer trim circuit, the trim circuit comprising:

a pair of trim latches, each storing a value representative of an enable signal, each trim latch connected to a respective enable input of one the first or the second stages to provide its enable signal to its respective output stage.

18. The output buffer of claim 17, wherein each of the first and the second stages further comprises:

a hard coded CMOS structure substantially identical to the first CMOS structure, the hard coded CMOS AND gate inputs connected to the data signal and to one of a plurality of hard coded enable signals, and the hard coded CMOS OR gate inputs connected to the data signal and to a complement of the one of the plurality of hard coded enable signals.

19. The output buffer of claim 18, and further comprising:

an output buffer enable selection circuit to select either the first and second stage CMOS structures or the hard coded CMOS structures.

20. The output buffer of claim 19, wherein the output buffer enable selection circuit comprises:

an OR gate having inputs connected to each of the enable latch output and a general enable signal, and having an output connected to the complement of the enable signal to enable a predetermined output buffer strength when either the enable latch output or the general enable signal are active, and to enable the trim latch enable signals when the enable latch output and the general enable signal are inactive.

21. A trim circuit for an output buffer having multiple parallel connected output stages, comprising:

a bank of latches, the bank of latches having an enable latch and a plurality of trim latches, each trim latch storing a value representative of an enable signal, each trim latch connected to a respective enable input of one of the output stages to provide its enable signal to its respective output stage; and

selection circuitry to select either the bank of latches or a preprogrammed enable signal.

22. The trim circuit of claim 21, wherein the selection circuitry comprises:

an OR gate having inputs connected to each of the enable latch output and a general enable signal, and having an output connected to the complement of the enable signal to enable a predetermined output buffer strength when either the enable latch output or the general enable signal are active, and to enable the trim latch enable signals when the enable latch output and the general enable signal are inactive.

23. A memory device, comprising:

an array of memory cells;

a plurality of data lines for access to the memory cells; and

an output buffer coupled between the array of memory cells and the plurality of data lines, wherein the output buffer comprises:

a first stage and a second stage, the first and second stages having outputs connected parallel to one another, the first stage providing buffer strength when a first stage enable signal is active, and the second stage providing buffer strength when a second stage enable signal is active.

24. The memory device of claim 23, wherein each output stage comprises:

a complementary metal oxide semiconductor (CMOS) structure having a p-channel MOS device and an n-channel MOS device;

an AND gate having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to a data signal and another input connected to one of a plurality of enable signals; and

an OR gate having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to the data signal and another input connected to a complement of the one of the plurality of enable signals.

25. The memory device of claim 23, wherein the output buffer further comprises:

a bank of latches, the bank of latches having an enable latch and two trim latches, each trim latch storing a value representative of an enable signal, each trim latch connected to the respective enable input of one the plurality of output stages to provide its enable signal to its respective output stage.

26. The memory device of claim 25, wherein each output stage further comprises:

a second CMOS structure substantially identical to the first CMOS structure, the second CMOS AND gate inputs connected to the data signal and to one of a plurality of hard coded enable signals, and the second CMOS OR gate inputs connected to the data signal and to a complement of the one of the plurality of hard coded enable signals.

27. The memory device of claim 26, wherein the output buffer further comprises:

an output buffer selection circuit, comprising an OR gate connected to the enable latch output and to a general enable signal, the OR gate output connected to the complement of the enable signal to enable a predetermined output buffer strength when either the enable latch output or the general enable signal are active.

28. The memory device of claim 23, and further comprising an output buffer trim circuit, the trim circuit comprising:

a bank of latches, the bank of latches having an enable latch and a plurality of trim latches, each trim latch storing a value representative of an enable signal,

each trim latch connected to a respective enable input of one the plurality of output stages to provide its enable signal to its respective output stage.

29. The memory device of claim 23, wherein the array of memory cells comprises an array of non-volatile memory cells.

30. A system, comprising:

a processor;

a memory device coupled to the processor, the memory device comprising:

an array of memory cells;

a plurality of data lines for access to the memory cells; and

an output buffer coupled between the array of memory cells and the plurality of data lines, wherein the output buffer comprises:

a first stage and a second stage, the first and second stages having outputs connected parallel to one another, the first stage providing buffer strength when a first stage enable signal is active, and the second stage providing buffer strength when a second stage enable signal is active.

31. The system of claim 30, wherein each output stage comprises:

a complementary metal oxide semiconductor (CMOS) structure having a p-channel MOS device and an n-channel MOS device;

an AND gate having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to a data signal and another input connected to one of a plurality of enable signals; and

an OR gate having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to the data signal and another input connected to a complement of the one of the plurality of enable signals.

32. The system of claim 30, wherein the output buffer further comprises:

a bank of latches, the bank of latches having an enable latch and two trim latches, each trim latch storing a value representative of an enable signal, each trim latch connected to the respective enable input of one the plurality of output stages to provide its enable signal to its respective output stage.

33. The memory device of claim 32, wherein each output stage further comprises:

a second CMOS structure substantially identical to the first CMOS structure, the second CMOS AND gate inputs connected to the data signal and to one of a plurality of hard coded enable signals, and the second CMOS OR gate inputs connected to the data signal and to a complement of the one of the plurality of hard coded enable signals.

34. The memory device of claim 33, wherein the output buffer further comprises:

an output buffer selection circuit, comprising an OR gate connected to the enable latch output and to a general enable signal, the OR gate output connected to the complement of the enable signal to enable a predetermined output buffer strength when either the enable latch output or the general enable signal are active.

35. A method of adjusting an output buffer strength, comprising:

selectively enabling at least one output buffer stage in response to a predetermined set of enable signals for the respective stages.

36. The method of claim 35, wherein selectively enabling comprises:

providing an enable signal to each of the at least one buffer stage, wherein each enable signal is stored in a latch; and

enabling each output stage for which its enable signal is active.

37. The method of claim 35, wherein selectively enabling at least one output buffer stage comprises:

providing a first enable signal to a first enable input of each of the output stages;

providing a second signal to a second enable input of each of the output stages; and

selecting between the first and the second enable signal and the selectable signal.

38. A method for adjusting a strength of an output buffer, comprising:

generating enable signals for a plurality of parallel output buffer stages;

enabling each stage having an enable signal; and

combining the strength of each enabled stage into a total buffer strength.

39. The method of claim 38, wherein combining the strength comprises connecting the plurality of output buffer stages in parallel.

40. The method of claim 38, wherein generating enable signals comprises:

programming a bank of trim latches with a plurality of values representative of enable signals; and

connecting an output of each trim latch to a respective output buffer stages.

41. A method of adjusting an output buffer strength, comprising:

selectively enabling at least one output buffer stage in response to a predetermined set of enable signals for the respective stages.

42. The method of claim 41, wherein each enabled output buffer stage contributes to a total strength of the output buffer.

43. The method of claim 41, wherein selectively enabling comprises:

providing an enable signal to each of the at least one buffer stage, wherein each enable signal is stored in a latch; and

enabling each output stage for which its enable signal is active.

44. The method of claim 41, wherein selectively enabling at least one output buffer stage comprises:

providing a first enable signal to a first enable input of each of the output stages;

providing a second signal to a second enable input of each of the output stages; and

selecting between the first and the second enable signal and the selectable signal.

45. A method of trimming an output buffer, comprising:

enabling at least one of a plurality of parallel connected output stages; and

combining a strength of each of the enabled output stages into a total output buffer strength.

46. A method of adjusting output buffer strength in a multiple stage output buffer, comprising:

selecting predetermined or programmable enable inputs for the output stages;

programming the programmable enable inputs when programmable enable inputs are selected; and

passing the predetermined enable inputs when predetermined enable inputs are selected.

47. A method of operating an integrated circuit, comprising:

programming a selectable input fuse to generate an active selectable input enable signal;

programming a predetermined enable signal set;

programming a selectable input set; and

selecting between the predetermined enable set and the selectable input set.

48. The method of claim 47, wherein selecting comprises:

combining in an OR gate the selectable input enable signal and an input select enable signal;

providing the selectable input set to a plurality of output buffer stages when the input select enable signal is active; and

providing the predetermined enable signal set when the input select enable signal is inactive.